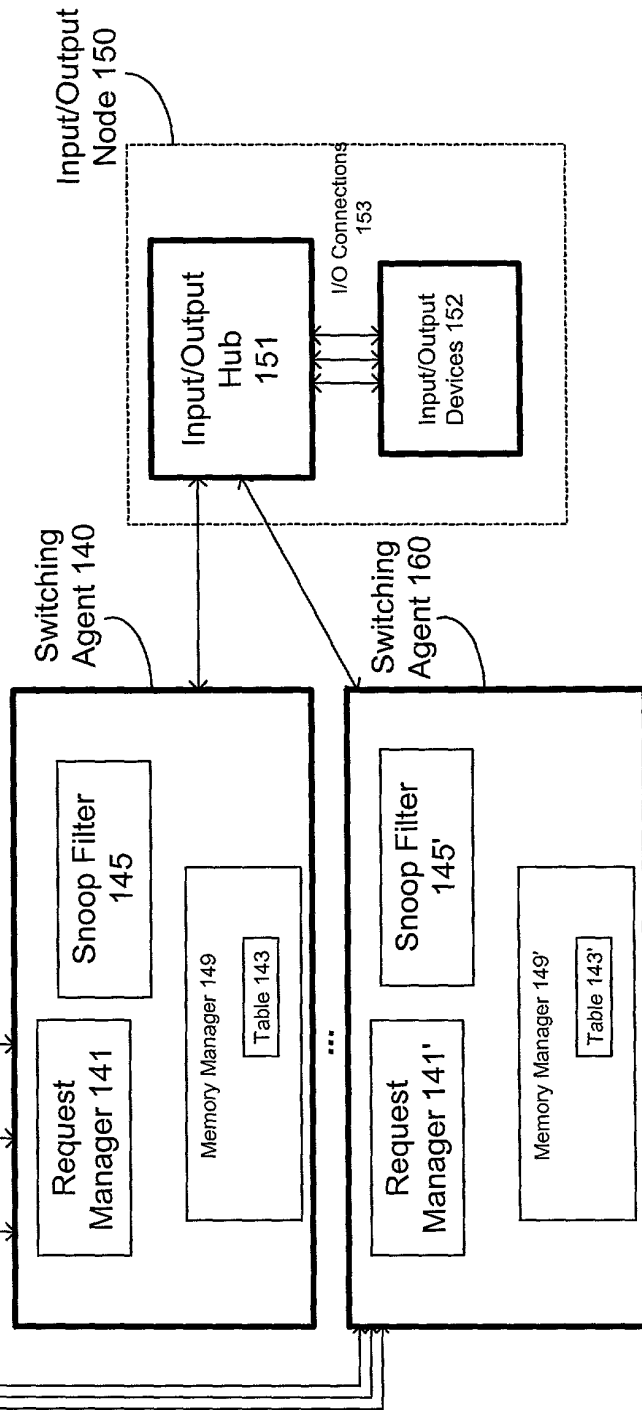
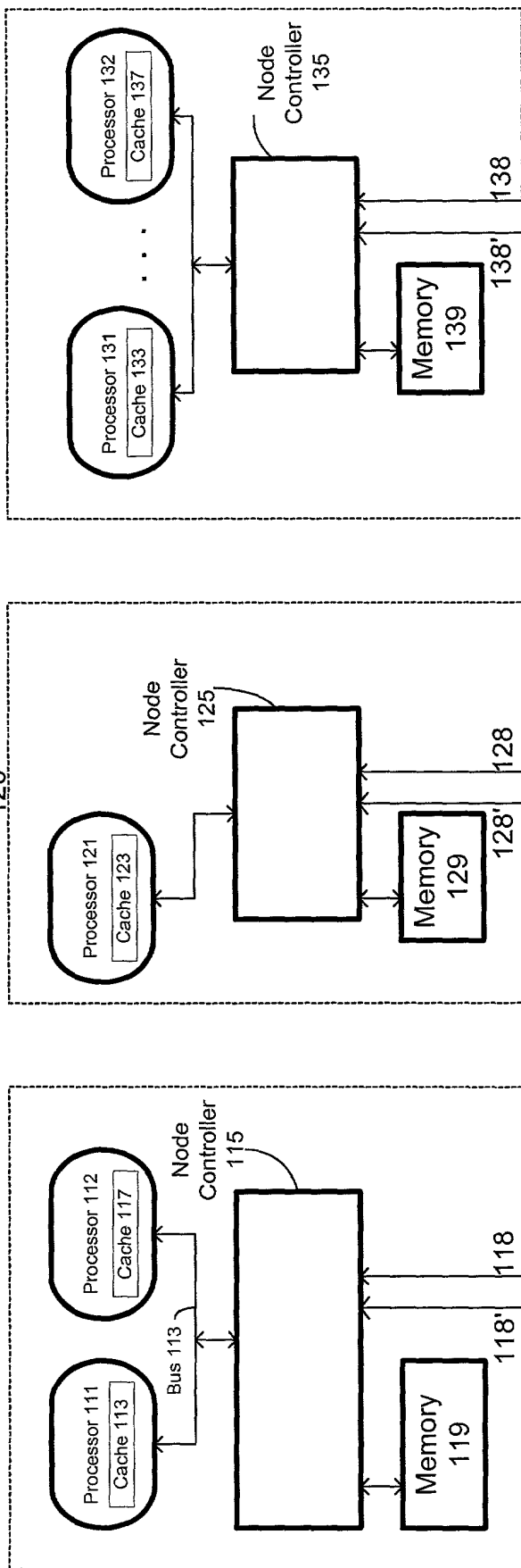


FIG. 1 is a block diagram of a system 100, including a first processor node 110, a second processor node 120, and a third processor node 130, each including a node controller, memory, and processors with caches. The system 100 also includes a switching agent 140 and an input/output node 150. The first processor node 110 includes a node controller 115, memory 119, and processors 111 and 112 with caches 113 and 117, respectively. The second processor node 120 includes a node controller 125, memory 129, and processor 121 with cache 123. The third processor node 130 includes a node controller 135, memory 139, and processors 131 and 132 with caches 133 and 137, respectively. The switching agent 140 includes a request manager 141, a snoop filter 145, and a memory manager 149 with table 143. The input/output node 150 includes an input/output hub 151 and input/output devices 152. The system 100 is connected via a bus 113 and various interconnects (118, 128, 138, 153) to the switching agent 140 and the input/output node 150.

First Processor Node 110

Second Processor Node 120

Third Processor Node 130



System 100

FIG. 1

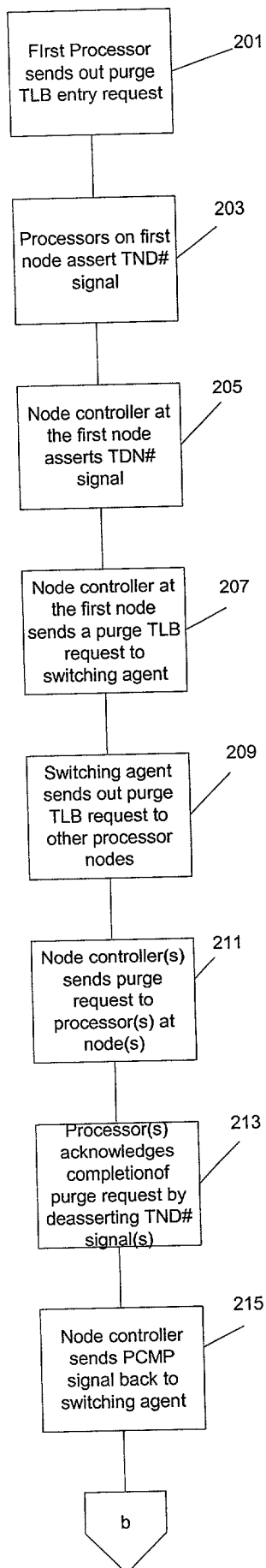


Fig 2a

